

GIGABYTE™

Z68X-UD3P-B3

Rev 1.0

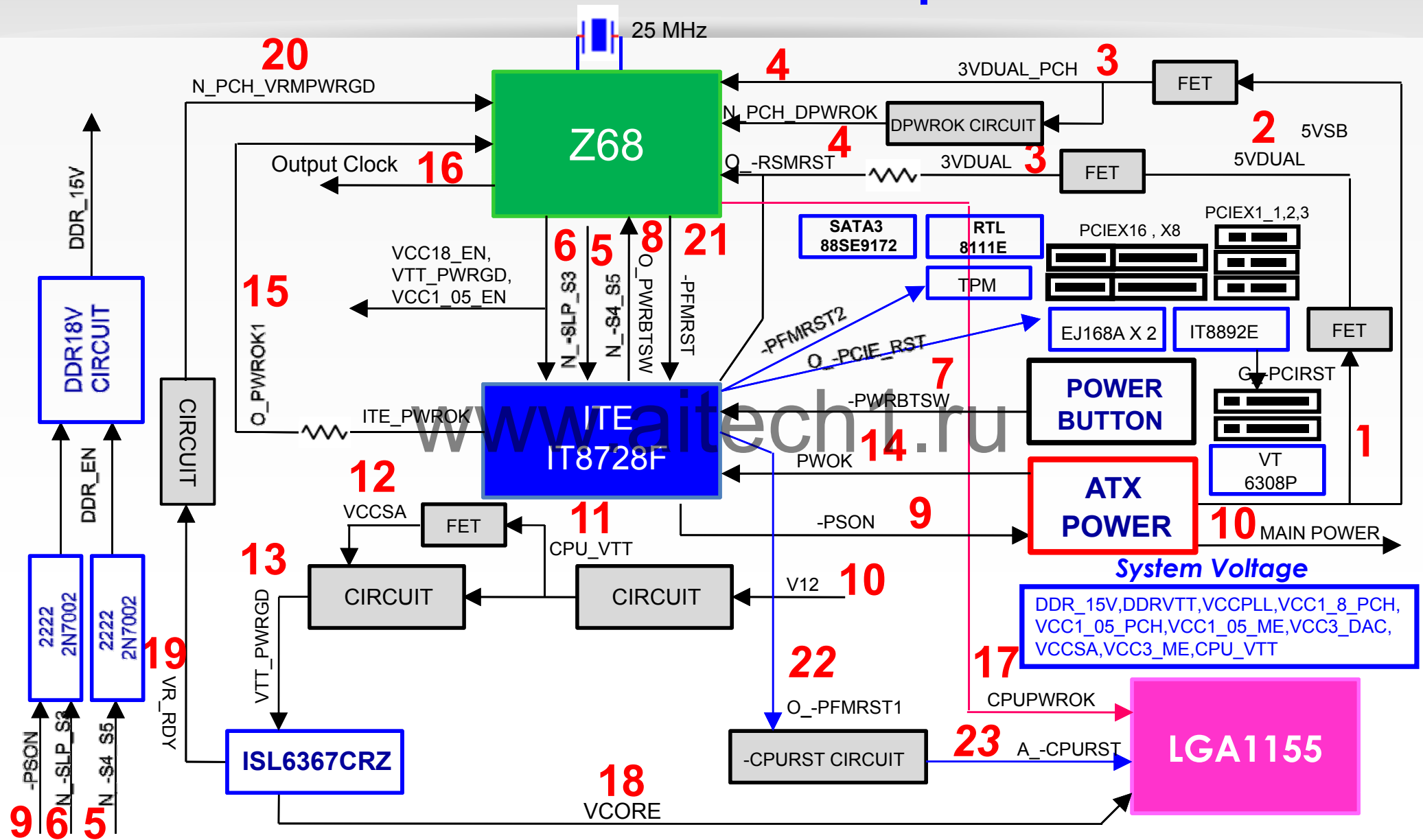
Power Sequence

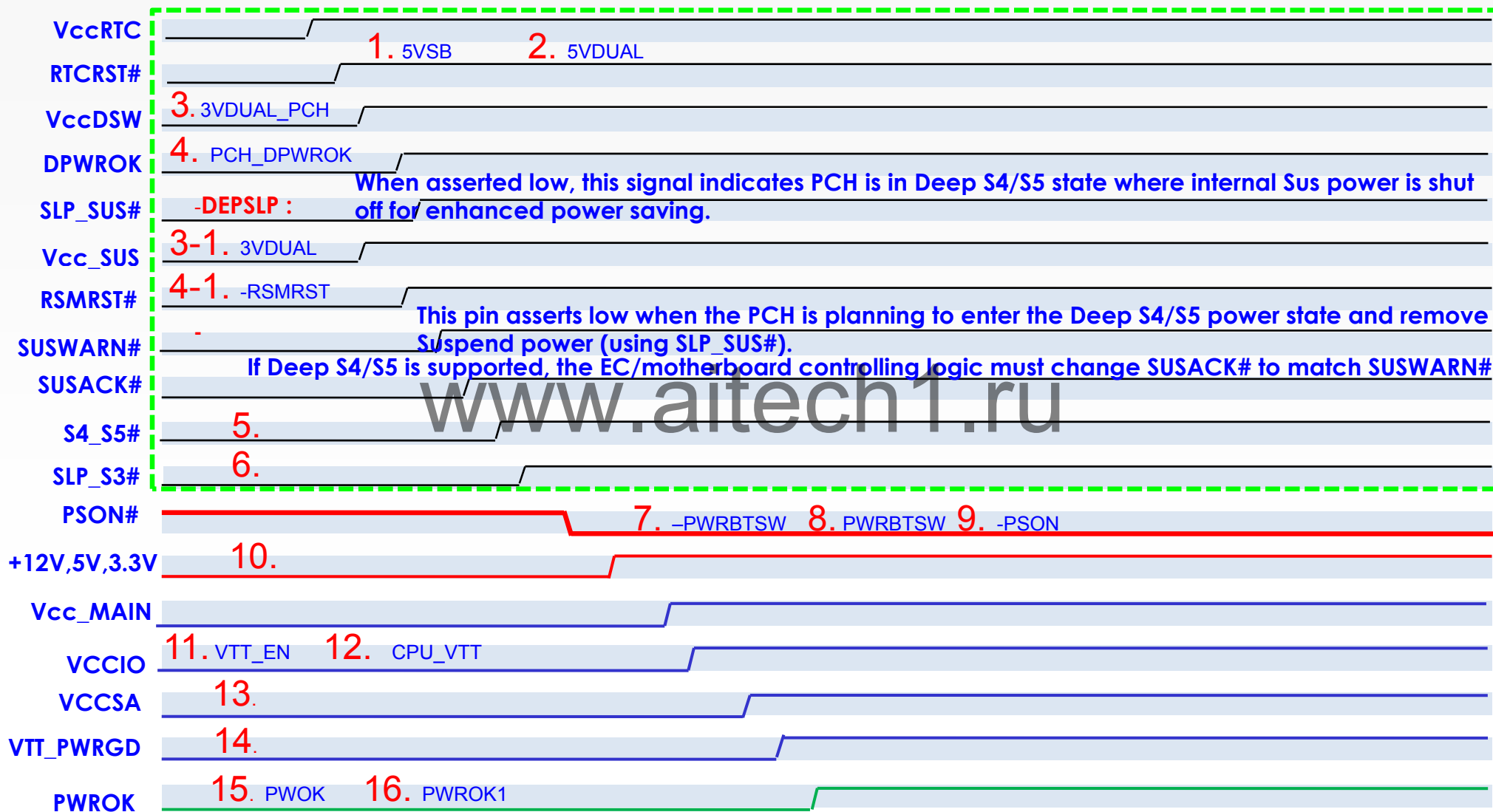
Signal Definition

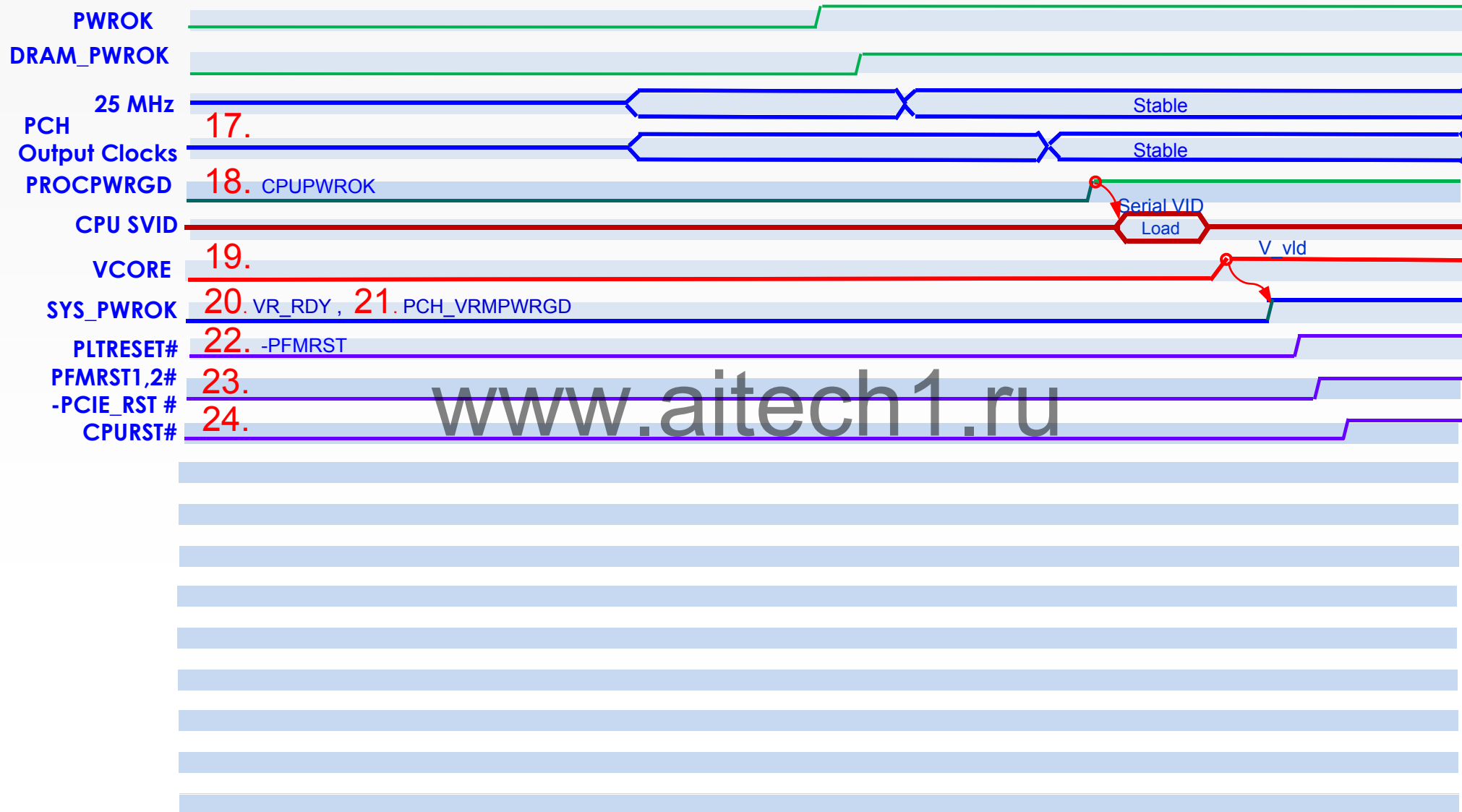
JEFF.KO



Z68X-UD3P-B3 Power Sequence







www.aitech1.ru

1155 CPU Sandy Bridge Processor
Signals Description
www.aitech1.ru

1155 CPU Sandy Bridge Processor Interface

System Memory Interface	System Memory Interface	Memory Reference and Compensation	Reset and Miscellaneous Signals	PCI Express* Graphics Interface Signals
Memory Channel A SA_BS[2:0] SA_WE# SA_RAS# SA_CAS# SA_DQ[8:0] SA_DQ#[8:0] SA_DQ[63:0] SA_MA[15:0] SA_CK[3:0] SA_CK#[3:0] SA_CKE[3:0] SA_CS#[3:0] SA_ODT[3:0]	Memory Channel B SB_BS[2:0] SB_WE# SB_RAS# SB_CAS# SB_DQ[8:0] SB_DQ#[8:0] SB_DQ[63:0] SB_MA[15:0] SB_CK[3:0] SB_CK#[3:0] SB_CKE[3:0] SB_CS#[3:0] SB_ODT[3:0]	SM_VREF	CFG[17:0] FC_x PM_SYNC RESET# SM_DRAMRST	PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RX[15:0] PEG_RX#[15:0] PE_RX[3:0]1 PE_RX#[3:0]1 PEG_TX[15:0] PEG_TX#[15:0] PE_TX[3:0]1 PE_TX#[3:0]1

Red : I/O put
 Blue : Output
 Green : Input

1155 CPU Sandy Bridge Processor Interface

Intel Flexible Display Interface	DMI - Processor to PCH Serial Interface	PLL Signals	TAP Signals	Error and Thermal Protection
FDI0_FSYNC[0] FDI0_LSYNC[0] FDI_TX[7:0] FDI_TX#[7:0] FDI1_FSYNC[1] FDI1_LSYNC[1] FDI_INT	DMI_RX[3:0] DMI_RX#[3:0] DMI_TX[3:0] DMI_TX#[3:0]	BCLK BCLK#	BPM#[7:0] BCLK_ITP BCLK_ITP# DBR# PRDY# PREQ# TCK TDI TDO TMS TRST#	CATERR# PECI PROCHOT# THERMTRIP#

www.aitech1.ru

Red : I/O put
 Blue : Output
 Green : Input

1155 CPU Sandy Bridge Processor Interface

Power Sequencing	Processor Power Signals	Sense Pins	Ground and NCTF	
SM_DRAMPWROK UNCOREPWRGOOD SKTOCC#	VCC VCCIO VDDQ VAXG VCCPLL VCCSA VIDSOUT VIDSCLK VIDALERT# VCCSA_VID	VCC_SENSE VSS_SENSE VAXG_SENSE VSSAXG_SENSE VCCIO_SENSE VSS_SENSE_VCCIO VDDQ_SENSE VSSD_SENSE VCCSA_SENSE	VSS VSS_NCTF (BGA only)	<div> Red : I/O put Blue : Output Green : Input </div>

Reset and Miscellaneous Signals

Signal Name	Description	Direction/ Buffer Type
CFG[17:0] :	Configuration Signals : The CFG signals have a default value of '1' if not terminated on the board. <ul style="list-style-type: none"> • CFG[1:0]: Reserved configuration lane. A test point may be placed on the board for this lane. • CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> — 1 = Normal operation — 0 = Lane numbers reversed • CFG[3]: Reserved • CFG[4]: Reserved configuration lane. A test point may be placed on the board for this lane. • CFG[6:5]: PCI Express Bifurcation: Note 1 <ul style="list-style-type: none"> — 00 = 1 x8, 2 x4 PCI Express — 01 = reserved — 10 = 2 x8 PCI Express — 11 = 1 x16 PCI Express • CFG[17:7]: Reserved configuration lanes. A test point may be placed on the board for these lands 	I CMOS
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands	
PM_SYNC	Power Management Sync : A sideband signal to communicate power management status from the platform to the processor	I CMOS
RESET#	Platform Reset pin driven by the PCH	I CMOS
SM_DRAM RST#	DDR3 DRAM Reset: Reset signal from processor to DRAM devices. One common to all channels.	O CMOS

PCI Express Based Interface Signals

Signal Name	Description	Direction/ Buffer Type
PEG_ICOMPI	PCI Express Input Current Compensation	I A
PEG_ICOMPO	PCI Express Current Compensation	I A
PEG_RCOMPO	PCI Express Resistance Compensation	I A
PEG_RX[15:0] PEG_RX#[15:0] PE_RX[3:0]1 PE_RX#[3:0]1	PCI Express Receive Differential Pair www.aitech1.ru	I PCI Express
PEG_TX[15:0] PEG_TX#[15:0] PE_TX[3:0]1 PE_TX#[3:0]1	PCI Express Transmit Differential Pair	O PCI Express

Intel Flexible Display Interface Signals

Signal Name	Description	Direction/ Buffer Type
FDI0_FSYNC[0]	Intel® Flexible Display Interface Frame Sync – Pipe A	I CMOS
FDI0_LSYNC[0]	Intel® Flexible Display Interface Line Sync – Pipe A	I CMOS
FDI_TX[7:0] FDI_TX#[7:0]	Intel® Flexible Display Interface Transmit Differential Pairs)	O FDI
FDI1_FSYNC[1]	Intel® Flexible Display Interface Frame Sync – Pipe B	I CMOS
FDI1_LSYNC[1]	Intel® Flexible Display Interface Line Sync – Pipe A	I CMOS
FDI_INT	Intel® Flexible Display Interface Hot Plug Interrupt	I Asynchronous CMOS

DMI- Processor to PCH Serial Interface

Signal Name	Description	Direction/ Buffer Type
DMI_RX[3:0] DMI_RX#[3:0]	DMI Input from PCH: Direct Media Interface receive differential pair.	I DMI
DMI_TX[3:0] DMI_TX#[3:0]	DMI Output to PCH: Direct Media Interface transmit differential pair.	O DMI

PLL Signals

Signal Name	Description	Direction/ Buffer Type
BCLK BCLK#	Differential bus clock input to the processor	I Diff Clk

TAP Signals

Signal Name	Description	Direction/ Buffer Type
BPM#[7:0]	Breakpoint and Performance Monitor Signals: These signals are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor Performance	I/O CMOS
BCLK_ITP BCLK_ITP#	These pins are connected in parallel to the top side debug probe to enable debug capacities.	I
DBR#	DBR# is used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset	O
PRDY#	PRDY# is a processor output used by debug tools to determine processor debug readiness.	O Asynchronous CMOS
PREQ#	PREQ# is used by debug tools to request debug operation of the processor.	I CMOS
TCK	TCK (Test Clock): This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). TCK must be driven low or allowed to float during power on Reset.	I CMOS
TDI	TDI (Test Data In): This signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I CMOS
TDO	TDO (Test Data Out): This signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O Open Drain
TMS	TMS (Test Mode Select): A JTAG specification support signal used by debug tools.	I CMOS
TRST#	TRST# (Test Reset): This signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	I CMOS

Error and Thermal Protection

Signal Name	Description	Direction/ Buffer Type
CATERR#	Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors	O CMOS
PECI	PECI (Platform Environment Control Interface): A serial sideband interface to the processor, it is used primarily for thermal, power, and error management	I/O Asynchronous
PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	CMOS Input/ Open-Drain Output
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous CMOS

Power Sequencing

Signal Name	Description	Direction/ Buffer Type
SM_DRAMPWROK	SM_DRAMPWROK Processor Input: Connects to PCH DRAMPWROK.	I Asynchronous CMOS
UNCOREPWRGOOD	The processor requires this input signal to be a clean indication that the VCCSA, VCCIO, VAXG, and VDDQ, power supplies are stable and within specifications.	I Asynchronous CMOS
SKTOCC#	SKTOCC# (Socket Occupied): Pulled down directly (0 Ohms) on the processor package to ground	

www.aitech1.ru

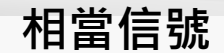
Processor Power Signals

Signal Name	Description	Direction/ Buffer Type
VCC	Processor core power rail	Ref
VCCIO	Processor power for I/O	Ref
VDDQ	Processor I/O supply voltage for DDR3	Ref
VAXG	Graphics core power supply.	Ref
VCCPLL	VCCPLL provides isolated power for internal processor PLLs	Ref
VCCSA	System Agent power supply	Ref
VIDSOUT VIDSCLK VIDALERT#	VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers. This serial VID interface replaces the parallel VID interface on previous processors.	I/O O I CMOS
VCCSA_VID	Voltage selection for VCCSA	O

Sense Pin

Signal Name	Description	Direction/ Buffer Type
VCC_SENSE VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VAXG_SENSE VSSAXG_SENSE	VAXG_SENSE and VSSAXG_SENSE provide an isolated, low impedance connection to the VAXG voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCIO_SENSE VSS_SENSE_VCCIO	VCCIO_SENSE and VSS_SENSE_VCCIO provide an isolated, low impedance connection to the processor VCCIO voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VDDQ_SENSE VSSD_SENSE	VDDQ_SENSE and VSSD_SENSE provides an isolated, low impedance connection to the VDDQ voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCSA_SENSE	VCCSA_SENSE provide an isolated, low impedance connection to the processor system agent voltage. It can be used to sense or measure voltage near the silicon.	O Analog

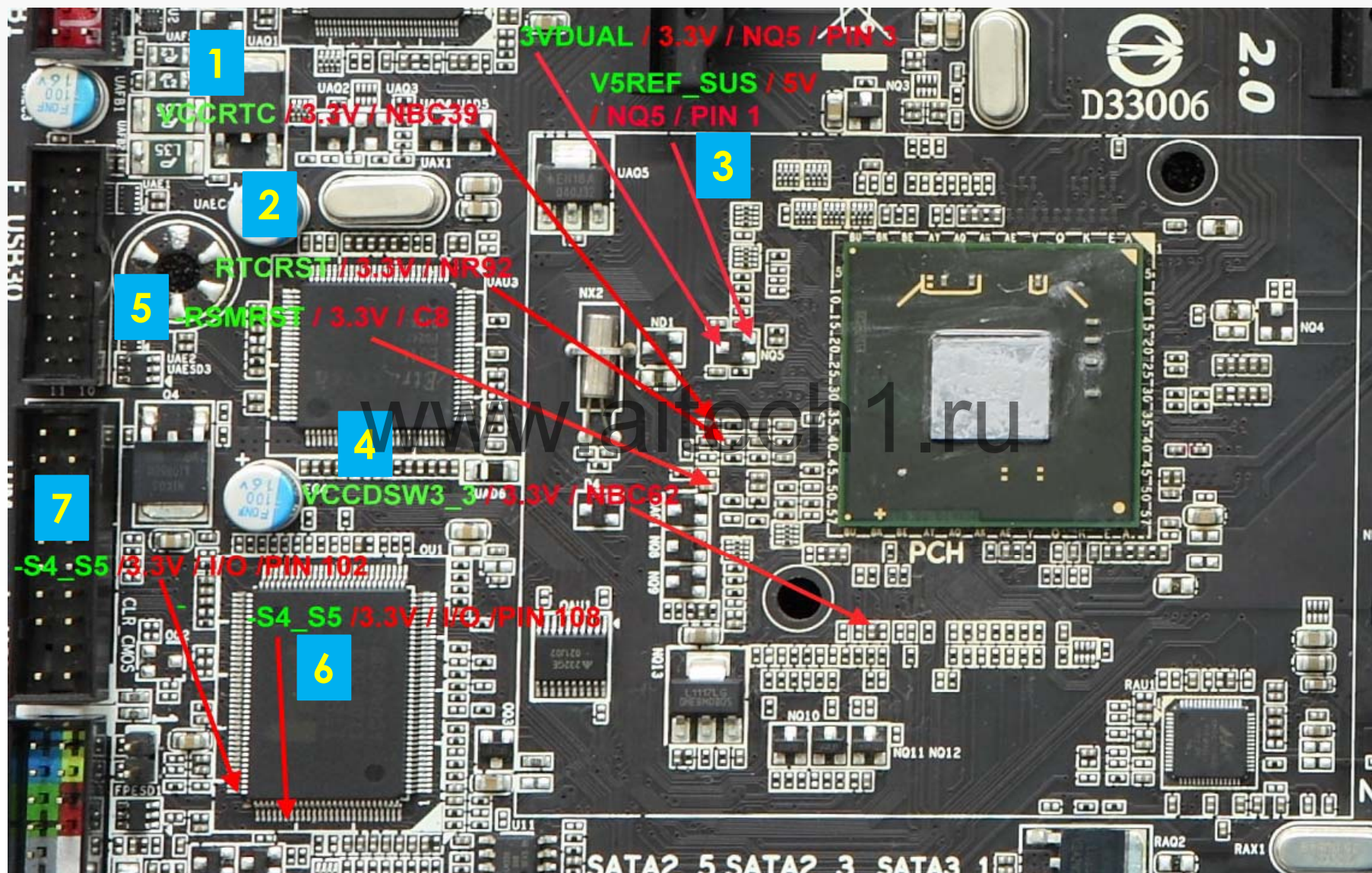
Z68



Intel Z68 Chip Before Power On Signals Sequence

Name 1	Name 2	Power	Location	Description
1. VCCRTC	N_RTCVDD	3.3V	NBC39	Supply for the RTC well.
2. -RTCRST	N_-RTCRST	3.3V	NR92	RTC Reset: When asserted, this signal resets register bits in the RTC well.
3. V5REF_SUS	5VDUAL / 3VDUAL	5V/3.3V	NQ5/PIN1/ PIN2,3	Reference for 5 V tolerance on suspend well inputs.
4. VccDSW3_3	3VDUAL_PC H	3.3V	NBC62	3.3 V supply for Deep S4/S5 wells
5. -RSMRST	O_-RSMRST	3.3V	C8	Resume Well Reset: This signal is used for resetting the resume power plane logic
6. -S4_S5	N_-S4_S5	3.3V	IO/PIN108	S4(Suspend to Disk) or S5 (Soft Off) state
7. -SLP_S3	N_-SLP_S3	3.3V	IO/PIN102	S3(Suspend To RAM)

Intel Z68 Chip Before Power On Check Point



Intel Z68 Chip Power On Signals Sequence

Name 1	Name 2	Power	Location	Description
1. V5REF	VCC/VCC3	5V / 3.3V	NQ3/PIN1/ PIN2,3	Reference for 5 V tolerance on core well inputs
2. VccASW VCCIO	VCC1_05_PCH VCC1_05_ME	1.05V	NBC8 NBC28	1.05 V supply for the Active Sleep Well 1.05 V supply for core well I/O buffers.
VCCDMI	CPU_VTT	1.0V	NBC43	Power supply for DMI
VCCVRM	VCC1_8_PCH	1.8V	NBC16	1.8 V supply for internal PLL and VRMs
VCCSPI	VCC3_ME	3.3V	NBC63	3.3 V supply for SPI Controller Logic
VCCA_DAC	VCC3_DAC	3.3V	NBC18	3.3 V supply for Display DAC Analog Power
VCC3_3	VCC3	3.3V	NBC12	3.3 V supply for core well I/O buffers.

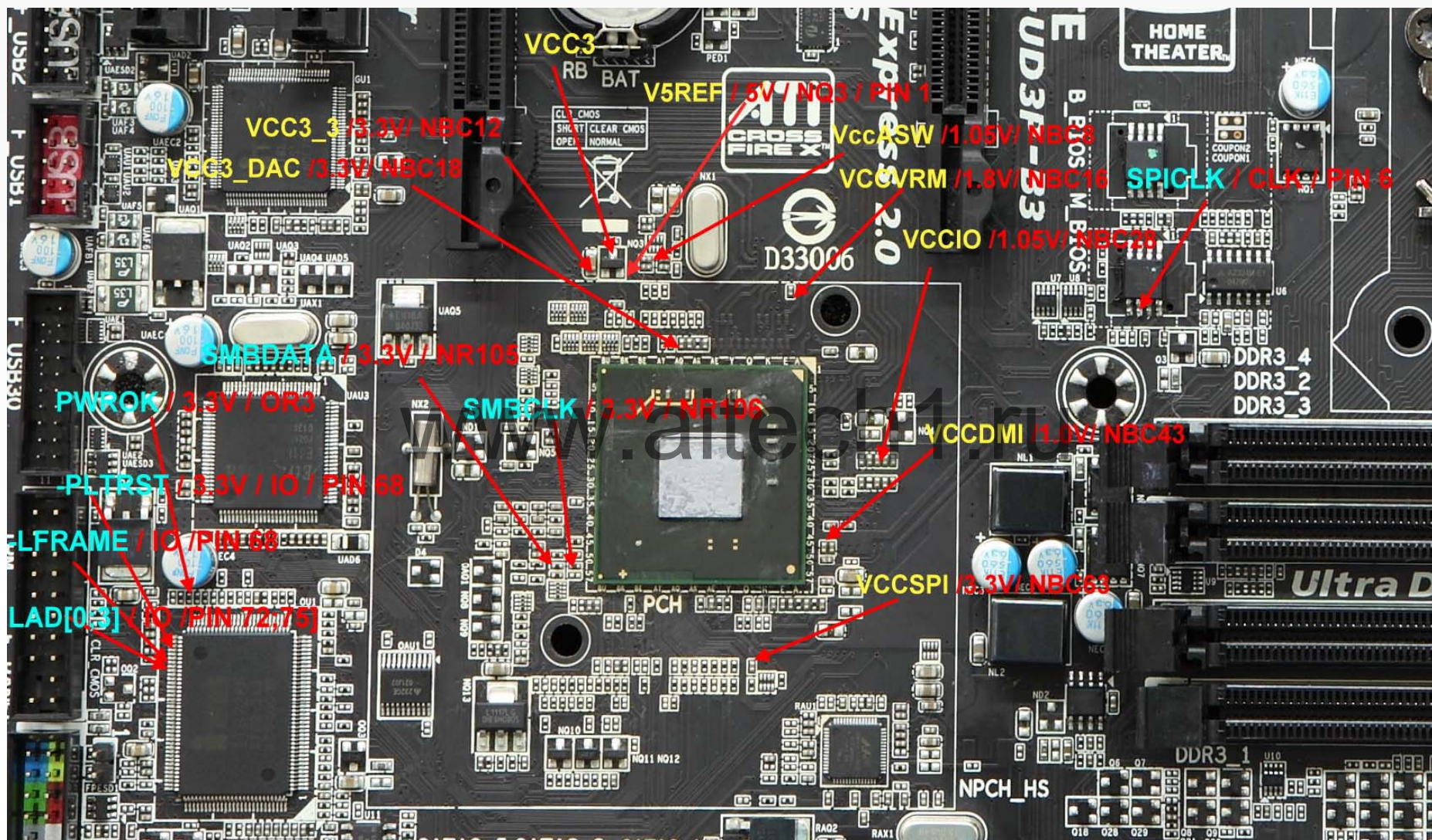
Intel Z68 Chip Power On Signals Sequence

Name 1	Name 2	Status	Location	Description
3. PWROK	O_PWROK1	3.3V	IO/PIN63/ OR3	Power OK: When asserted, PWROK is an indication to the Cougar Point that all of its core power rails have been stable for 10 ms.
APWROK	O_APWROK1	3.3V	SAME	Active Sleep Well (ASW) Power OK: When asserted, indicates that power to the ASW sub-system is stable.
4. CLKOUT_DMI_N CLKOUT_DMI_P	N_CUCLK N_CPUCLK	CLK	LED tool	100-MHz PCIe Gen2 specification jitter tolerant differential output to processor.
5. PROCPWRGD	N_CPUPWROK	1V	LED tool	Processor Power Good: This signal should be connected to the processor's UNCOREPWRGOOD input to indicate when the processor power is valid.
6. SYS_PWROK	N_PCH_VRMPWRGD	3.3V	DQ81/PIN 3	SYS_PWROK is used to inform the Cougar Point that power is stable to some other system component(s) and the system is ready to start the exit from reset.
7. -PLTRST	N_PFMIRST	3.3V	IO/PIN68	Platform Reset: The Cougar Point asserts PLTRST# to reset devices on the platform.
8. DMI[0;3]TXN DMI[0;3]RXN	A_DMI_[0;3]TXN A_DMI_[0;3]RXN		LED tool	Direct Media Interface

Intel Z68 Chip Power On Other Signals

Name 1	Name 2	Status	Location	Description
SMBCLK SMBDATA	SMBDATA SMBCLK	3.3V	NR105/DDR SK NR106/DDR SK	SMBus Clock SMBus Data
LFRAME	N_-LFRAME	SIGNAL	IO/PIN71	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LAD[0;3]	N_LAD[0;3]	SIGNAL	IO/PIN[:75]72	LPC Multiplexed Command, Address, Data: For LAD[3:0],
SPI_CLK	N_ICH_SPI_CLK	CLK	BIOS/PIN6	SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

Intel Z68 Chip Power On Check Point



Z68 Interface Signals

<u>1. DMI</u>	9. LPC Interface	16. SMBus Interface
2. PCI-E	10. AUDIO	17. Power Mgnt
3. USB	11. SPI	18. Misc Signals
4. Intel Flexible Display Interface	12. RTC	19. Interrupt Interface
5. FAN Speed Control	13. SMB	20. Clock Inputs/Outputs
6. General Purpose IO	14. JTAG	21. Processor Interface
7. SATA2	15. System Mgnt	22. Power
8. SATA3		

Z68 Cougar Point Interface
Signals Definition
www.aitech1.ru

Z68 Cougar Point Interface

PCI Interface	Processor Interface	SPI	LPC Interface	Clock Outputs
AD[31:0] C/BE[3:0]# DEVSEL# FRAME# IRDY# TRDY# STOP# PAR PERR# REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54 GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55 SERR# PME# CLKIN_PCILoopBACK PCIRST# PLOCK#	PMSYNCH RCIN# A20GATE THRMPTRIP# PROCPWRGD	SPI_CS0#; SPI_CS1# SPI_MISO SPI_MOSI SPI_CLK	LAD[3:0]/FWH[3:0] LFRAME#/FWH4 LDRQ0#; LDRQ1#/GPIO23	CLKOUT_DP_[P,N] CLKOUT_DMI_[P,N] XTAL25_OUT CLKOUT_PEG_A_[P,N];CLK OUT_PEG_B_[P,N] CLKOUT_PCIE[7:0]_[P,N] CLKOUT_ITPXD_[P,N] CLKOUT_PCI[4:0] CLKOUTFLEX0/GPIO64;CL KOUTFLEX1/GPIO65 CLKOUTFLEX2/GPIO66;CL KOUTFLEX3/GPIO67

Red : I/O put
Blue : Output
Green : Input

Z68 Cougar Point Interface

Clock Inputs	Interrupt Interface	USB	RTC	Misc Signals
CLKIN_DMI_[P,N]; CLKIN_DMI2_[P,N] CLKIN_SATA_[P,N]/ CKSSCD_[P,N] CLKIN_DOT96[P,N] XTAL25_IN;REF14CLKIN PCIECLKRQ0#/GPIO73; PCIECLKRQ1#/GPIO18 PCIECLKRQ2#/GPIO20/SMI#; PCIECLKRQ3#/GPIO25 PCIECLKRQ4#/GPIO26; PCIECLKRQ5#/GPIO44 PCIECLKRQ6#/GPIO45; PCIECLKRQ7#/GPIO46 PEG_A_CLKRQ#/GPIO47; PEG_B_CLKRQ#/GPIO56 XCLK_RCOMP	SERIRQ PIRQ[D:A]# PIRQ[H:E]#/GPIO[5:2]	USB[13:0][P,N] OC0#/GPIO59; OC1#/GPIO40 OC2#/GPIO41; OC3#/GPIO42 OC4#/GPIO43; OC5#/GPIO9 OC6#/GPIO10; OC7#/GPIO14 USBRBIAS, USBRBIAS#	RTCX1 RTCX2	INTVRMEN, DSWVRMEN SPKR SRTCST#; RTCST# INIT3_3V# TPn GPIO35/NMI# GPIO24/PROC_MISSING

www.aitech1.ru

Red : I/O put
 Blue : Output
 Green : Input

General Purpose I/O	Fan Speed Control	Intel Flexible Display	Controller Link	PCI Express Interface
GPIO[72,57,32,28,27,15,8]	PWM[3:0] TACH7/GPIO71;TACH6/GPIO70; TACH5/GPIO69;TACH4/GPIO68 TACH3/GPIO7; TACH2/GPIO6; TACH1/GPIO1;TACH0/GPIO17 SST PECI	FDI_RX[P,N][7:4] FDI_RX[P,N][3:0] FDI_FSYNC[0:1];FDI_LSYNC[0:1];FDI_INIT	CL_CLK1 ; CL_DATA1 CL_RST1#	PET[p,n][8:1] PER[p,n][8:1]

Red : I/O put
Blue : Output
Green : Input

Serial ATA Interface	Power Mngt	Intel High Definition Audio	Direct Media Interface	SMBus Interface
SATA[5:0]TX[P,N] SATA[5:0]RX[P,N] SATAICOMPO, SATA3COMPO SATAICOMPI, SATA3COMPI SATA3RBIAS SATALED# SATA0GP/GPIO21 SATA1GP/GPIO19 SATA2GP/GPIO36 SATA3GP/GPIO37 SATA4GP/GPIO16 SATA5GP/GPIO49/ TEMP_ALERT# SCLOCK/GPIO22, SLOAD/GPIO38 SDATAOUT0/GPIO39, SDATAOUT1/GPIO48	SUSWARN#/SUS_PWR_ DN_ACK/GPIO30 DPWROK SYS_RESET# RSMRST# SLP_S3# SLP_S4# SLP_S5#/GPIO63 SLP_A# CLKRUN#/GPIO32 PWROK AWROK PWRBTN# RI# WAKE# SUS_STAT#/GPIO61 SUSCLK/GPIO62 BATLOW#/GPIO72 PLTRST# BMBUSY#/GPIO0 STP_PCI#/GPIO34 ACPRESENT/GPIO31 DRAMPWROK LAN_PHY_PWR_CTRL/ GPIO12 SLP_LAN#/GPIO29 SUSACK#	HDA_RST# HDA_SYNC HDA_BCLK HDA_SDO HDA_SDIN[3:0] HDA_DOCK_EN#;HDA_D OCK_RST#	DMI[3:0]TX[P,N] DMI[3:0]RX[P,N] DMI_ZCOMP DMI_IRCOMP	SMBDATA; SMBCLK SMBALERT#/GPIO11

Red : I/O put
 Blue : Output
 Green : Input

System Mgmt	Analog Display	LVDS	Digital Display Interface	JTAG
INTRUDER#; SML[1:0]DATA;SML[1:0]CLK SML0ALERT#/GPIO60 SML1ALERT#/PCHHOT#/GPIO74	CRT_RED;CRT_GREEN; CRT_BLUE DAC_IREF CRT_HSYNC;CRT_VSYNC NC CRT_DDC_CLK;CRT_DDC_DATA DC_DATA CRT_IRTN	LVDS[A:B]_DATA[3:0] LVDS[A:B]_DATA#[3:0] LVDS[A:B]_CLK;LVDS[A:B]_CLK# LVD_VREFH;LVD_VREFL; LVD_VBG LVD_IBG L_DDC_CLK;L_DDC_DATA L_VDDEN;L_BLKTEN;L_BLKCTL	DDPB_[3:0][P,N] DDPC_[3:0][P,N] DDPD_[3:0][P,N] DDP[B:D]_AUX[P,N] DDP[B:D]_HPD SDVO_CTRLCLK;SDVO_CTRLDATA DDPC_CTRLCLK;DDPC_CTRLDATA DDPD_CTRLCLK;DDPD_CTRLDATA SDVO_INT[P,N] SDVO_TVCLKIN[P,N] SDVO_STALL[P,N]	JTAGTCK JTAGTMS JTAGTDI JTAGTDO

Red : I/O put
Blue : Output
Green : Input

Power and Ground Signals

Power and Ground				
DcpRTC DcpSST DcpSus DcpSusByp V5REF V5REF_Sus VccCore Vcc3_3 VccASW VccDMI VccDIFFCLKN VccRTC VccIO VccSus3_3 VccSus3_3 VccSusHDA VccVRM VccDFTERM VccADPLLA VccADPLLB VccADAC VccAClk VccAPLLEXP VccAPLLDMI2 VccAFDIPLL VccAPLLSATA V_PROC_IO VccDSW3_3`	VccSPI VccSSC VccClkDMI			

www.aitech1.ru

Red : I/O put
Blue : Output
Green : Input

Power and Ground Signals

Name	Power	Description
DcpRTC	CAP pull low	Decoupling: This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	CAP pull low	Decoupling: Internally generated 1.5 V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	2 CAP pull low TP	1.05 V Suspend well power. Internal VR mode (INTVRMEN sampled high): Well generated internally. Pins should be left No Connect External VR mode (INTVRMEN sampled low): Well supplied externally. Pins should be powered by 1.05 Suspend power supply. Decoupling capacitors are required. NOTE: External VR mode applies to Mobile Only.
DcpSusByp	TP	Internally generated 1.05 V Deep S4/S5 well power. This rail should not be supplied externally. NOTE: No decoupling capacitors should be used on this rail.
V5REF	VCC/VCC3	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	5VDUAL/3VDUAL	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	VCC1_05_PCH	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	VCC3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccASW	VCC1_05_ME	1.05 V supply for the Active Sleep Well. Provides power to the Intel® ME and integrated LAN. This plane must be on in S0 and other times the Intel ME or integrated LAN is used.

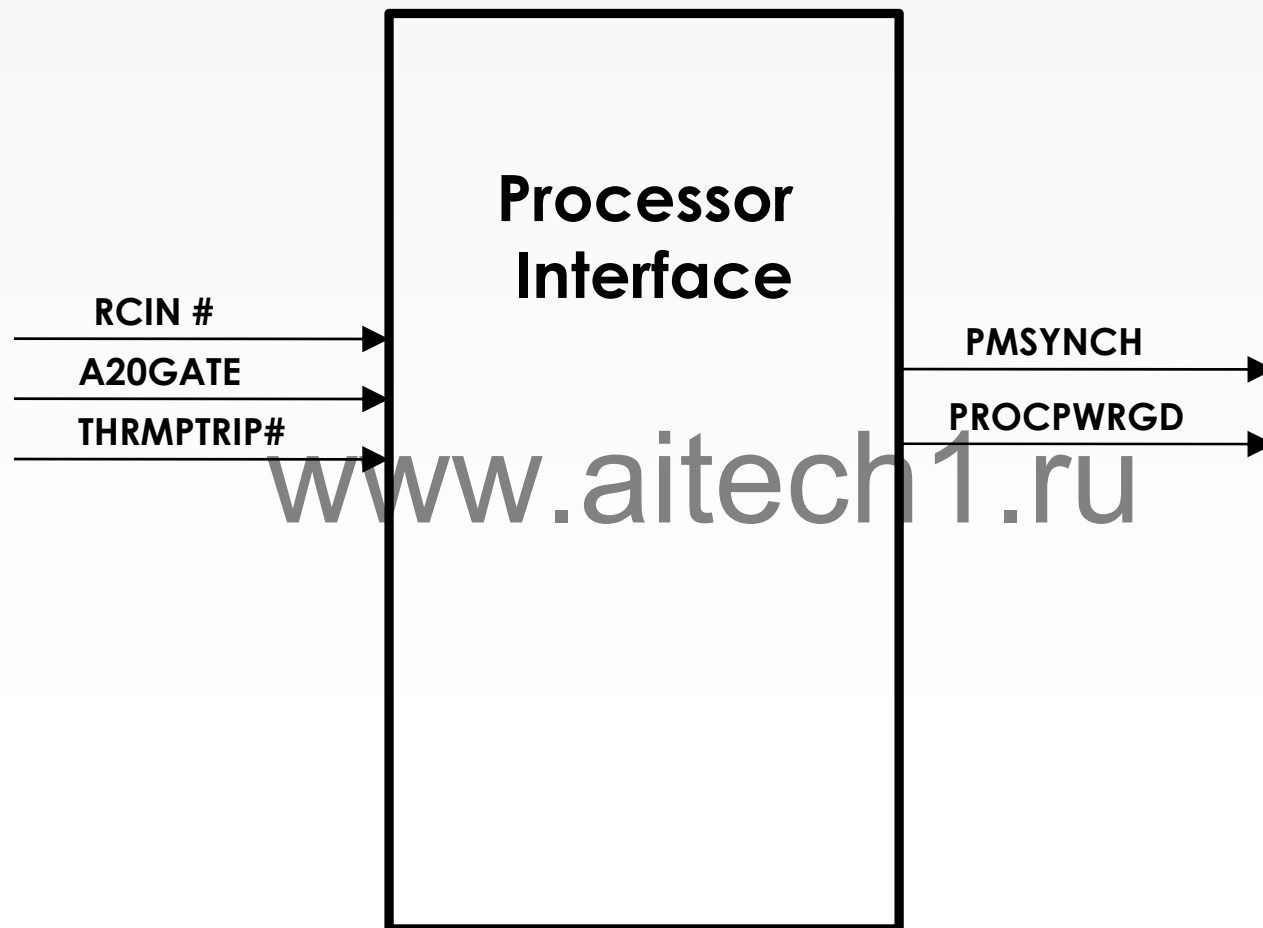
Power and Ground Signals

Name	Power	Description
VccDMI	CPU_VTT	Power supply for DMI. 1.1 V or 1.05 V based on the processor used. Please refer to the respective processor documentation to find the appropriate voltage level.
VccDIFFCLKN	VCC1_05_PCH	1.05 V supply for Differential Clock Buffers. This power is supplied by the corewell.
VccRTC	RTCVDD	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. NOTE: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VccIO	VCC1_05_PCH	1.05 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3VDUAL	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccSusHDA	3VDUAL	Suspend supply for Intel® HD Audio. This pin can be either 1.5 or 3.3 V.
VccVRM	VCC1_8_PCH	1.5 V/1.8 V supply for internal PLL and VRMs
VccDFTERM	VCC1_8_PCH	1.8 V or 3.3 V supply for DF_TV5. This pin should be pulled up to 1.8 V or 3.3 V core.
VccADPLLA	VCC1_05_PCH	1.05 V supply for Display PLL A Analog Power. This power is supplied by the core well.
VccADPLLB	VCC1_05_PCH	1.05 V supply for Display PLL B Analog Power. This power is supplied by the core well.
VccADAC	VCC3_DAC	3.3 V supply for Display DAC Analog Power. This power is supplied by the core well.

Power and Ground Signals

Name	Power	Description
VccAClk	NC	1.05 V Analog power supply for internal clock PLL. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLEXP	NC	1.05 V Analog Power for DMI. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLDMI2	NC	1.05 V Analog Power for internal PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAFDIPLL	NC	1.05 V analog power supply for the FDI PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAPLLSATA	NC	1.05 V analog power supply for SATA PLL. This power is supplied by core well. This rail requires an LC filter when power is supplied from an external VR. NOTE: This pin can be left as no connect
V_PROC_IO	CPU_VTT	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals. Please refer to the respective processor documentation to find the appropriate voltage level.
<u>VccDSW3_3</u>	3VDUAL_PCH	3.3 V supply for Deep S4/S5 wells. If platform does not support Deep S4/S5 then tie to VccSus3_3.
VccSPI	VCC3_ME	3.3 V supply for SPI Controller Logic. This rail must be powered when VccASW is powered. NOTE: This rail can be optionally powered on 3.3 V Suspend power (VccSus3_3) based on platform needs.
VccSSC	VCC1_05_PCH	1.05 V supply for Integrated Clock Spread Modulators. This power is supplied by core well.
VccClkDMI	VCC1_05_PCH	1.05 V supply for DMI differential clock buffer

Processor Interface



Processor Interface

Name	Type	Description
RCIN#	I	Keyboard Controller Reset Processor : The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the PCH's other sources of INIT#. When the PCH detects the assertion of this signal, INIT# is generated using a VLW message to the processor. NOTE: The PCH will ignore RCIN# assertion during transitions to the S3, S4, and S5 states
A20GATE	I	A20 Gate: A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# VLW message to the Processor active.
PROCPWRGD	○	Processor Power Good: This signal should be connected to the processor's UNCOREPWRGOOD input to indicate when the processor power is valid.
PMSYNCH	○	Power Management Sync: Provides state information from the PCH to the Processor
THRMTRIP#	I	Thermal Trip: When low, this signal indicates that a thermal trip from the processor occurred, and the Cougar Point will immediately transition to a S5 state. The Cougar Point will not wait for the processor stop grant cycle since the processor has overheated.

Virtual Legacy Wire (VLW) Messages

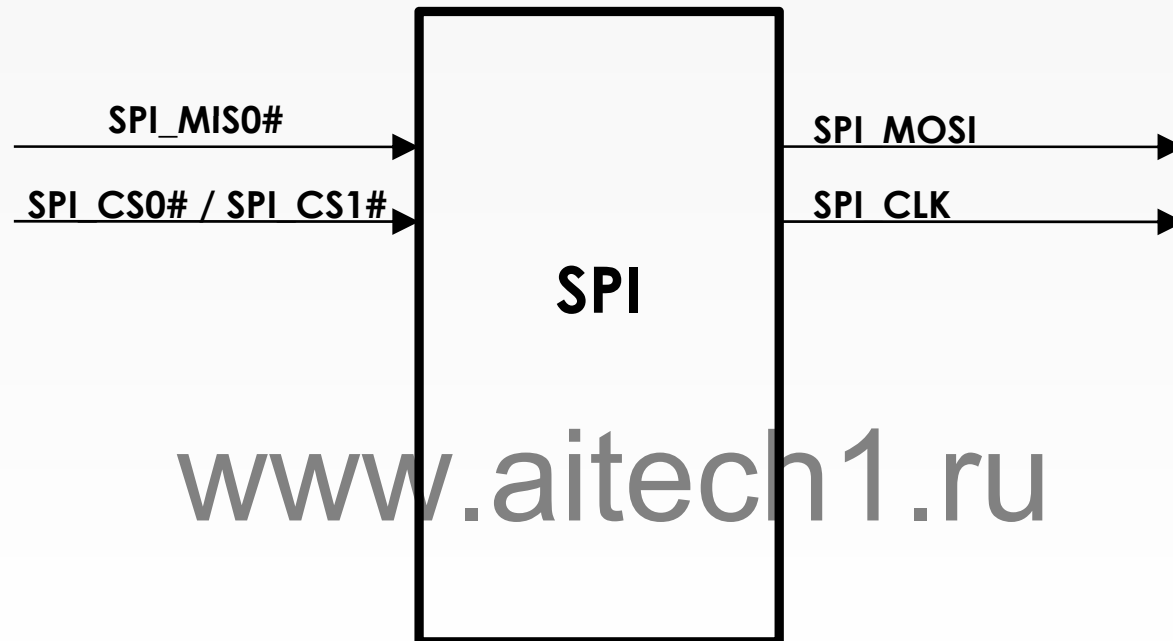
The PCH supports VLW messages as alternative method of conveying the status of the following legacy sideband interface signals to the processor :

- A20M#, INTR, SMI#, INIT#, NMI

Note: IGNNE# VLW message is not required to be generated by the PCH as it is Internally emulated by the processor.

VLW are inbound messages to the processor .**They are communicated using Vendor Defined Message over the DMI link**
Legacy processor signals can only be delivered using VLW in the PCH. Delivery of legacy processor signals (A20M#, INTR, SMI#, INIT# or NMI) using I/O APIC controller is not supported.

SPI Interface Signals

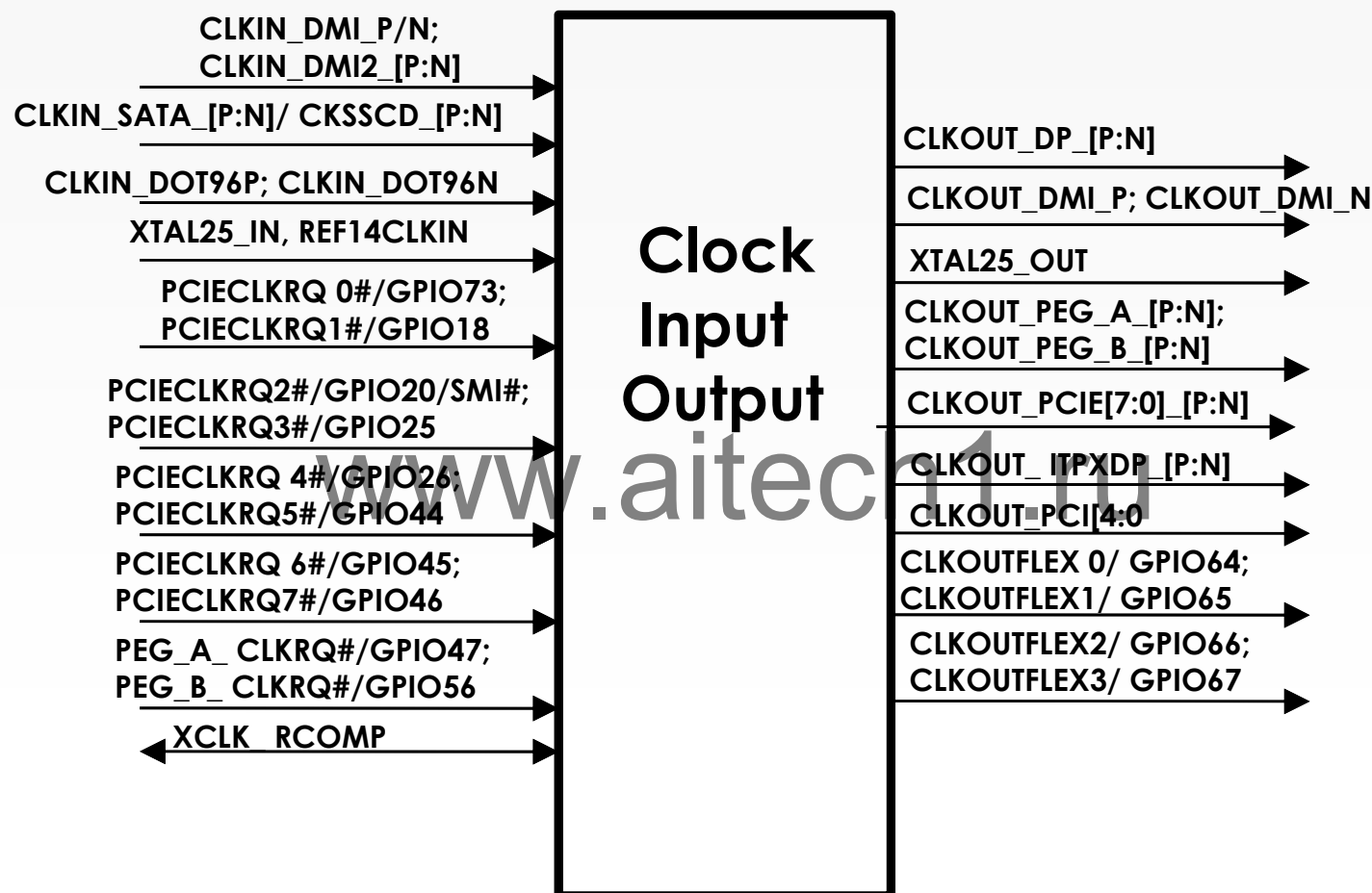


Serial Peripheral Interface (SPI) Signals Definition

Name	Type	Description
SPI_CS0#	O	SPI Chip Select 0: Used as the SPI bus request signal .
SPI_CS1#	O	SPI Chip Select 1: Used as the SPI bus request signal .
SPI_MISO	I	SPI Master IN Slave OUT: Data input pin for Z68.
SPI_MOSI	O	SPI Master OUT Slave IN: Data output pin for Z68.
SPI_CLK	O	SPI Clock: SPI clock signal , during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

www.aitech1.ru

Clock Interface



Clock Interface Signals

Name	Type	Description
CLKOUT_ITPXD_P CLKOUT_ITPXD_N	○	100-MHz Differential output to Processor XDP/ITP connector on platform
CLKOUT_DP_P , CLKOUT_DP_N	○	120-MHz Differential output for DisplayPort reference
CLKIN_DMI_P , CLKIN_DMI_N	I	100-MHz PCIe* Gen2 specification jitter tolerant differential reference clock from a clock chip in Buffer-Through Mode.
CLKOUT_DMI_P , CLKOUT_DMI_N	○	100-MHz PCIe Gen2 specification jitter tolerant differential output to processor.
CLKIN_SATA_P , CLKIN_SATA_N	I	100-MHz differential reference clock from a clock chip, provided separately from CLKIN_DMI, for use only as a 100-MHz source for SATA.
CLKIN_DOT96_P , CLKIN_DOT96_N	I	96-MHz differential reference clock from a clock chip. Unused when Integrated Clock Generation is enabled.
XTAL25_IN	I	Connection for 25-MHz crystal to Cougar Point oscillator circuit.
XTAL25_OUT	○	Connection for 25-MHz crystal to Cougar Point oscillator circuit.
REFCLK14IN	I	Single-ended 14.31818-MHz reference clock driven by a clock chip.

Clock Interface Signals

Name	Type	Description
CLKOUT_PEG_A_P, CLKOUT_PEG_A_N	O	100-MHz Gen2 PCIe specification differential output to PCI Express Graphics device
CLKOUT_PEG_B_P, CLKOUT_PEG_B_N	O	100-MHz Gen2 PCIe specification differential output to a second PCI Express Graphics device
PEG_A_CLKRQ# /GPIO47 (mobile only), PEG_B_CLKRQ# / GPIO56 (mobile only)	I	Clock Request Signals for PCIe Graphics SLOTS Can instead by used as GPIOs
CLKOUT_PCIE[7:0]_P, CLKOUT_PCIE[7:0]_N	O	100-MHz PCIe Gen2 specification differential output to PCI Express devices
CLKIN_GND0_P, CLKIN_GND0_N (Desktop Only) CLKIN_GND1_P, CLKIN_GND1_N	I	Requires external pull-down termination (can be shared between P and N signals of the differential pair). Unused in Integrated Clock Mode & Buffer Through Mode.
PCIECLKRQ0# /GPIO73, PCIECLKRQ1# /GPIO18, PCIECLKRQ3# /GPIO25, PCIECLKRQ4# /GPIO26 (all the above CLKRQ# signals are mobile only)	I	Clock Request Signals for PCI Express 100-MHz Clocks Can instead by used as GPIOs
PCIECLKRQ2# / GPIO20 / SMI#, PCIECLKRQ5# / GPIO44, PCIECLKRQ6# / GPIO45, PCIECLKRQ7# / GPIO46	I	Clock Request Signals for PCI Express 100-MHz Clocks Can instead by used as GPIOs

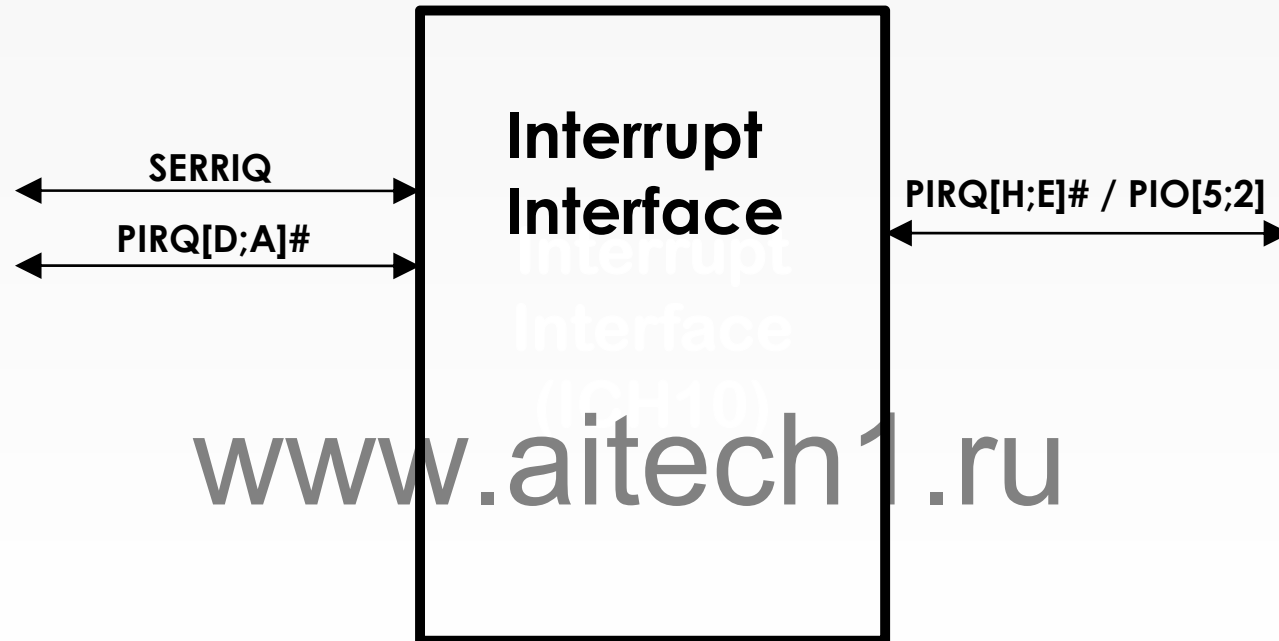
Clock Interface Signals

Name	Type	Description
CLKOUT_PCI[4:0]	○	Single-Ended, 33-MHz outputs to PCI connectors/devices.
CLKIN_PCILOOPBACK	I	33 MHz PCI clock feedback input, to reduce skew between PCH on-die PCI clock and PCI clock observed by connected PCI devices
CLKOUTFLEX0¹ / GPIO64	○	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: <ul style="list-style-type: none"> • 33 MHz • 27 MHz (SSC/Non-SSC) • 48/24 MHz • 14.318 MHz • DC Output logic '0'
CLKOUTFLEX1¹ / GPIO65	○	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: <ul style="list-style-type: none"> • Non functional and unsupported clock output value (Default) • 27MHz (SSC/Non-SSC) • 14.318 MHz output to SIO/EC • 48/24 MHz • DC Output logic '0'
CLKOUTFLEX2¹ / GPIO66	○	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: <ul style="list-style-type: none"> • 33 MHz • 25MHz • 27 MHz (SSC/Non-SSC) • 48/24 MHz • 14.318 MHz • DC Output logic '0'

Clock Interface Signals

Name	Type	Description
CLKOUTFLEX3¹ / GPIO67	○	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: <ul style="list-style-type: none"> • 27MHz (SSC/Non SSC) • 14.318 MHz output to SIO • 48/24 MHz (Default) • DC Output logic '0'
XCLK_RCOMP	I/O	Differential clock buffer Impedance Compensation: Connected to an external precision resistor ($90.9\ \Omega \pm 1\%$) to VccDIFFCLKN

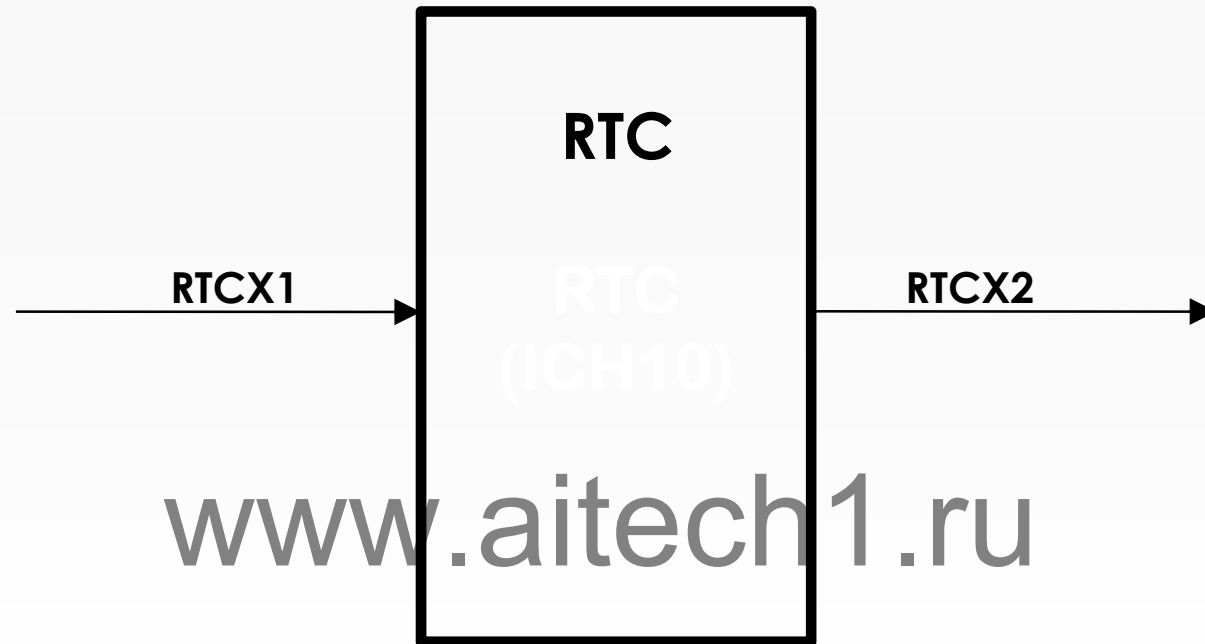
Interrupt Interface Signals



Interrupt Interface Signals Definition

Name	Type	Description
SERIRQ	IDO	Serial Interrupt Request: This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/DO	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/DO	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees The legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.

Real Time Clock

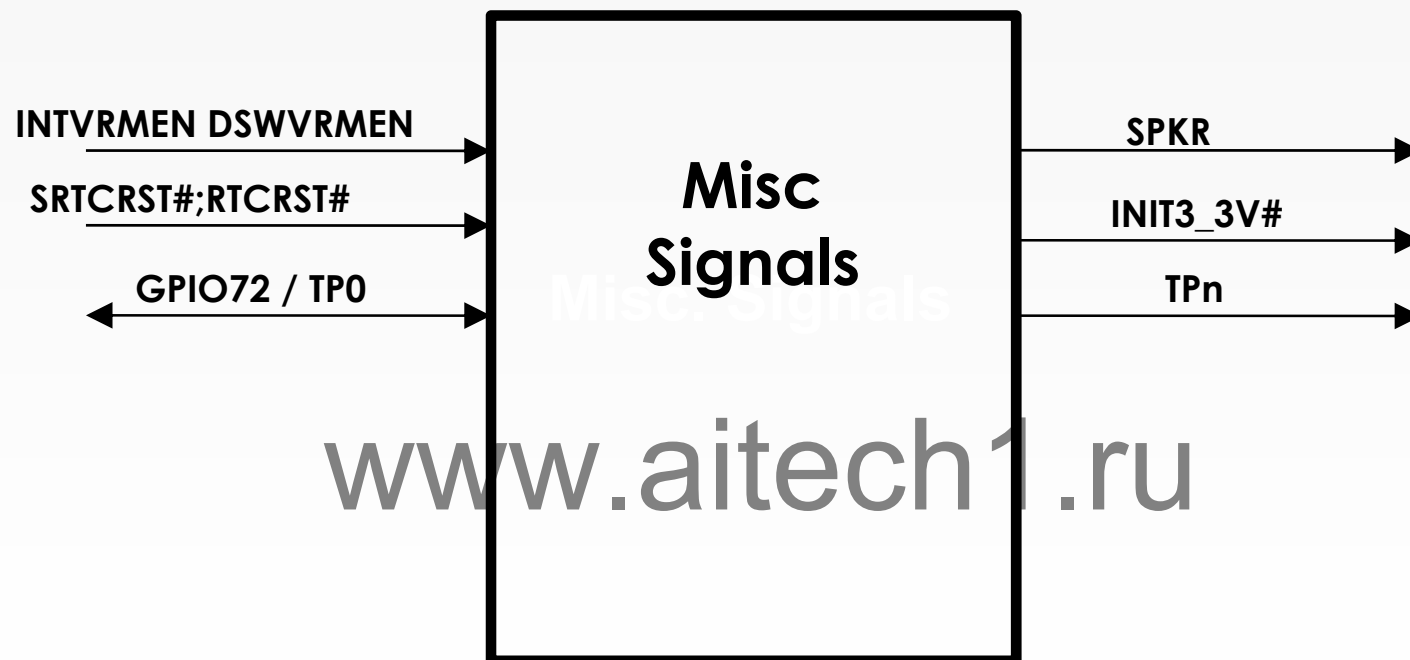


Real Time Clock Interface Definition

Name	Type	Description
RTCX1	special	Crystal Input 1: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	special	Crystal Input 2: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

www.aitech1.ru

Misc. Signals



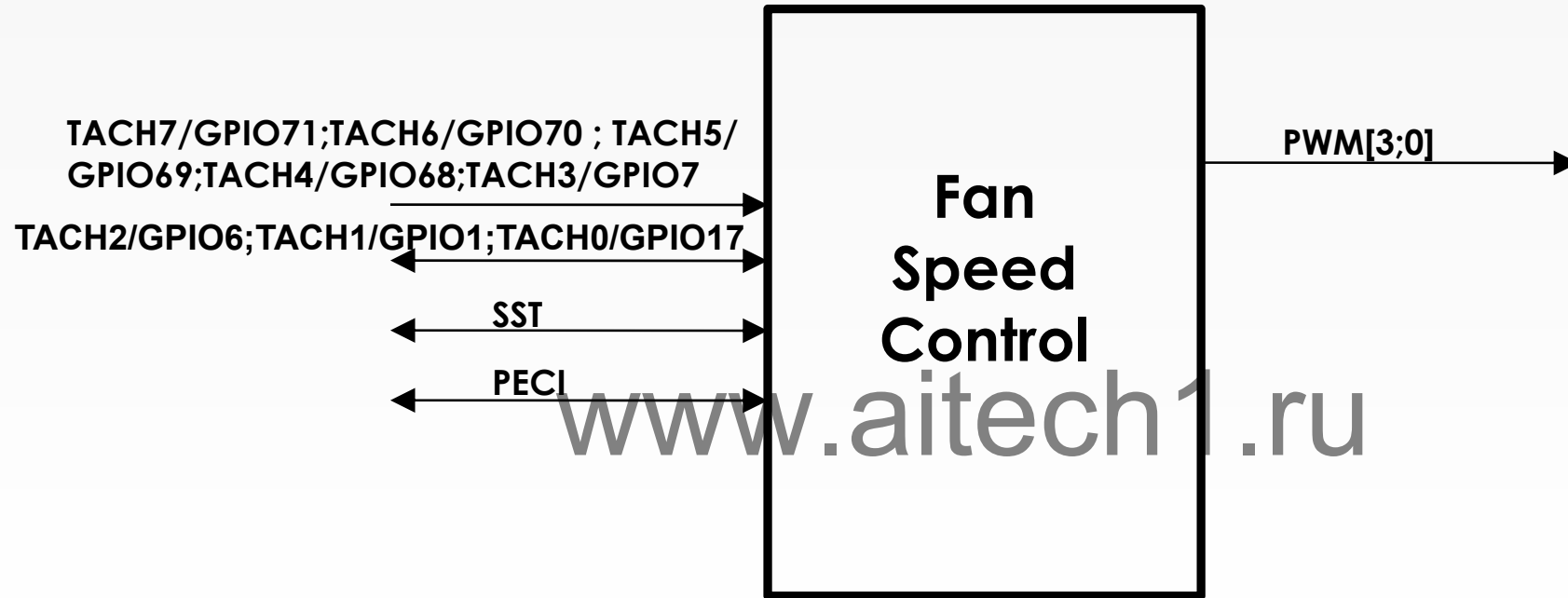
Miscellaneous Signals Definition

Name	Type	Description
SRTCST#	I	<p>Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The SRTCST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCST# pin must rise before the RSMRST# pin.
RTCST#	I	<p>RTC Reset: When asserted, this signal resets register bits in the RTC well.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCST# pin must rise before the RSMRST# pin.
INTVRMEN	I	<p>Internal Voltage Regulator Enable: This signal enables the internal VccSus1_1, VccSus1_5 and VccCL1_5 regulators. This signal must be pulled-up to VccRTC.</p>
DSWVRMEN	I	<p>Deep S4/S5 Well Internal Voltage Regulator Enable: This signal enables the internal DSW 1.05 V regulators. This signal must be always pulled-up to VccRTC</p>

Miscellaneous Signals Definition

Name	Type	Description
SPKR	○	Speaker: The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h Bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker.
SML1ALERT#/ PCHHOT#/ GPIO74	OD	PCHHOT#: This signal is used to indicate a PCH temperature out of bounds condition to an external EC, when PCH temperature is greater than value programmed by BIOS. An external pull-up resistor is required on this signal.
INIT3_3V#	○	Initialization 3.3 V: INIT3_3V# is asserted by the Cougar Point for 16 PCI clocks to reset the processor. This signal is intended for Firmware Hub.

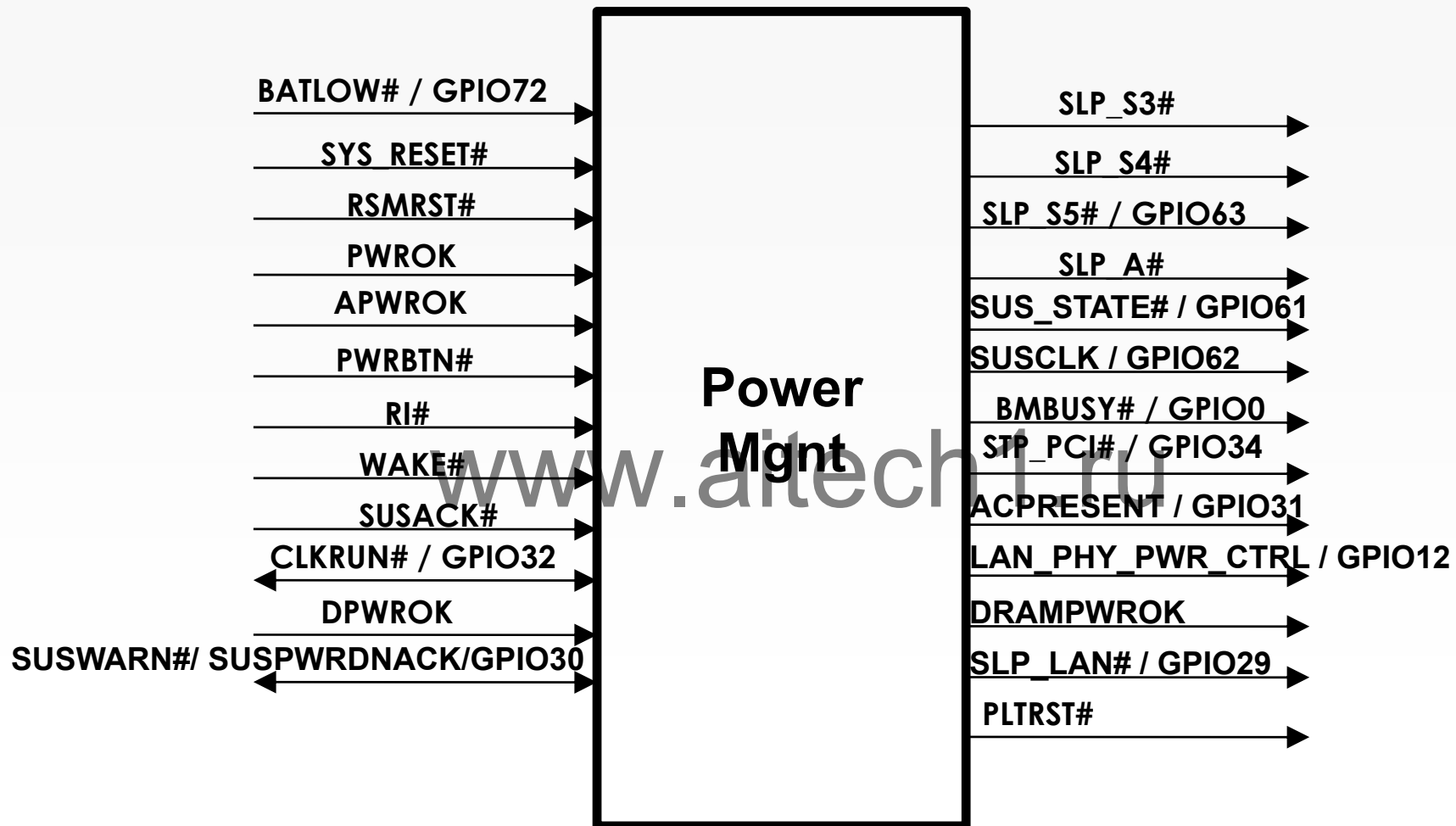
Fan Speed Control Signals



Thermal Signals

Name	Type	Description
PWM[3:0] (Server Usage Only); Not available in Mobile & Desktop)	OD ○	Fan Pulse Width Modulation Outputs: Pulse Width Modulated duty cycle output signals used for fan control. These signals are 5 V tolerant.
TACH0 / GPIO17 TACH1 / GPIO1 TACH2 / GPIO6 TACH3 / GPIO7 TACH4 / GPIO68 TACH5 / GPIO69 TACH6 / GPIO70 TACH7 / GPIO71 (TACH* signals used on Server Only; not available in Mobile & Desktop)	I	Fan Tachometer Inputs: Tachometer pulse input signal that is used to measure fan speed. This signal is connected to the "Sense" signal on the fan. Can instead be used as a GPIO.
SST (Server Usage Only; not available in Mobile & Desktop)	I/○	Simple Serial Transport: Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors.
PECI	I/○	Platform Environment Control Interface: Single-wire, serial bus.

Power Management Interface



Power Management Interface Definition

Name	Type	Description
ACPRESENT / GPIO31	I	ACPRESENT: This input pin indicates when the platform is plugged into AC power or not.
APWROK	I	Active Sleep Well (ASW) Power OK: When asserted, indicates that power to the ASW sub-system is stable.
BATLOW# (Mobile Only) / GPIO72	O	Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S3–S5 state. This signal can also be enabled to cause an SMI# when asserted. NOTE: Desktop requires a weak external pull-up.
BMBUSY# / GPIO0	I	Bus Master Busy: Generic bus master activity indication driven into the PCH. Can be configured to set the PM1_STS.BM_STS bit. Can also be configured to assert indications transmitted from the PCH to the Processor via the PMSYNCH pin.
CLKRUN# (Mobile Only) / GPIO32 (Desktop Only)	I/O	PCI Clock Run: Used to support PCI CLKRUN protocol. Connects to peripherals that need to request clock restart or prevention of clock stopping.

Power Management Interface Definition

Name	Type	Description
<u>DPWROK</u>	I	DPWROK: Power OK Indication for the VccDSW3_3 voltage rail. This input is tied together with RSMRST# on platforms that do not support Deep S4/S5. This signal is in the RTC well.
<u>DRAMPWROK</u>	OD ○	DRAM Power OK: This signal should connect to the Processor's SM_DRAMPWROK pin. The PCH asserts this pin to indicate when DRAM power is stable.
LAN_PHY_PWR_CTRL / GPIO12	○	LAN PHY Power Control: LAN_PHY_PWR_CTRL should be connected to LAN_DISABLE_N on the PHY. Cougar Point will drive LAN_PHY_PWR_CTRL low to put the PHY into a low power state when functionality is not needed.
PWROK	I	Power OK: When asserted, PWROK is an indication to the Cougar Point that all of its core power rails have been stable for 10 ms. PWROK can be driven asynchronously. When PWROK is negated, the Cougar Point asserts PLTRST#.

Power Management Interface Definition

Name	Type	Description
PLTRST#	○	Platform Reset: The Cougar Point asserts PLTRST# to reset devices on the platform.
PWRBTN#	I	Power Button: The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state.
RI#	I	Ring Indicate: This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures
SYS_RESET#	I	System Reset: This pin forces an internal reset after being Debounced. The Ibex Peak will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms \pm 2 ms for the SMBus to idle before forcing a reset on the system.
WAKE#	I	PCI Express* Wake Event: Sideband wake signal on PCI Express asserted by components requesting wake up.
<u>-RSMRST#</u>	I	Resume Well Reset: This signal is used for resetting the resume power plane logic. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable.
<u>SLP_A#</u>	○	SLP_A#: used to control power to the active sleep well (ASW) of the PCH.
<u>SLP_LAN#</u> / GPIO29	○	LAN Sub-System Sleep Control: When SLP_LAN# is deasserted it indicates that the PHY device must be powered. When SLP_LAN# is asserted power can be shut off to the PHY device.

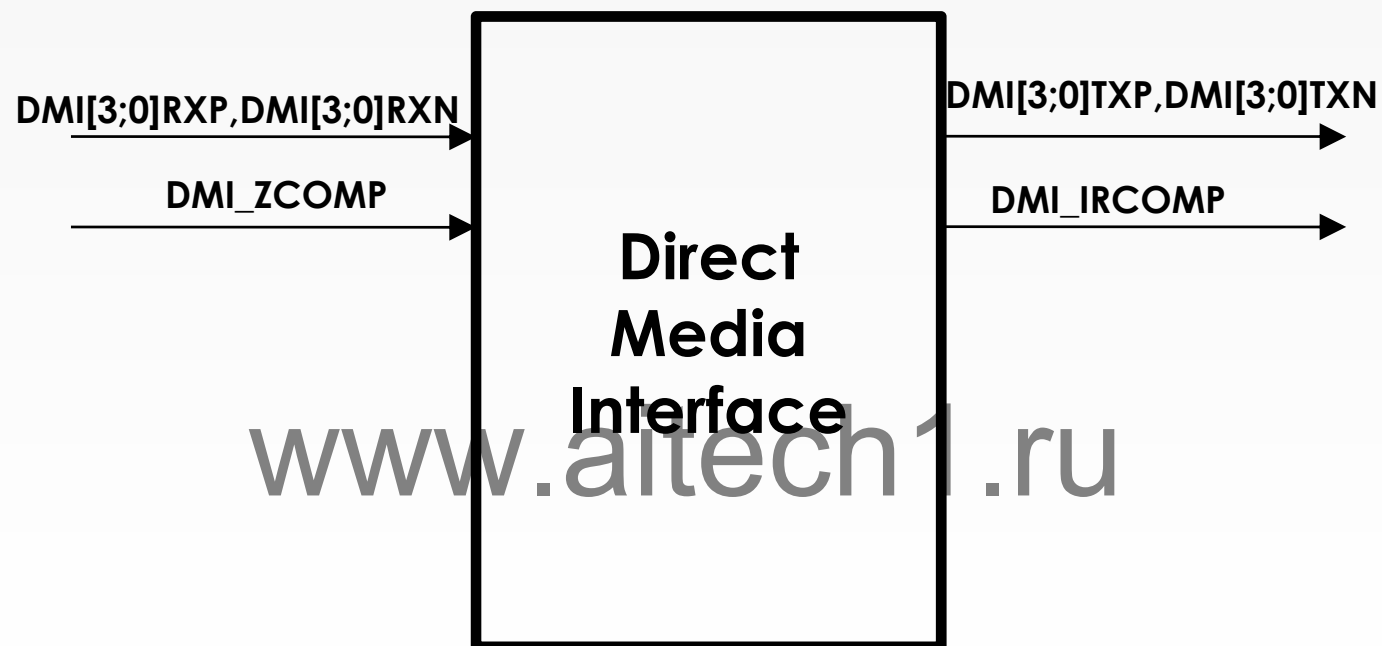
Power Management Interface Definition

Name	Type	Description
SLP_S3#	○	S3 Sleep Control: SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	○	S4 Sleep Control: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state
SLP_S5# / GPIO63	○	S5 Sleep Control: SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states. Pin may also be used as GPIO63.
<u>SLP_SUS#</u>	○	Deep S4/S5 Indication: When asserted low, this signal indicates PCH is in Deep S4/S5 state where internal Sus power is shut off for enhanced power saving. If Deep S4/S5 is not supported, then this pin can be left unconnected. This pin is in the DSW power well.
STP_PCI# / GPIO34	○	Stop PCI Clock: This signal is an output to the clock generator for it to turn off the PCI clock.
SUSACK#	I	SUSACK#: If Deep S4/S5 is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.
<u>SUS_STAT# / GPIO61</u>	○	Suspend Status: This signal is asserted by the Cougar Point to indicate that the system will be entering a low power state soon.

Power Management Interface Definition

Name	Type	Description
<u>SUSCLK /</u> GPIO62	O	Suspend Clock: This clock is an output of the RTC generator circuit to use by other chips for refresh clock. Pin may also be used as GPIO62.
SUSWARN# / SUSPWRDNACK / GPIO30	O	SUSWARN#: This pin asserts low when the PCH is planning to enter the Deep S4/S5 power state and remove Suspend power (using SLP_SUS#).
SYS_PWROK	I	System Power OK: This generic power good input to the Cougar Point is driven and utilized in a platform-specific manner. While PWROK always indicates that the core wells of the Cougar Point are stable, SYS_PWROK is used to inform the Cougar Point that power is stable to some other system component(s) and the system is ready to start the exit from reset.

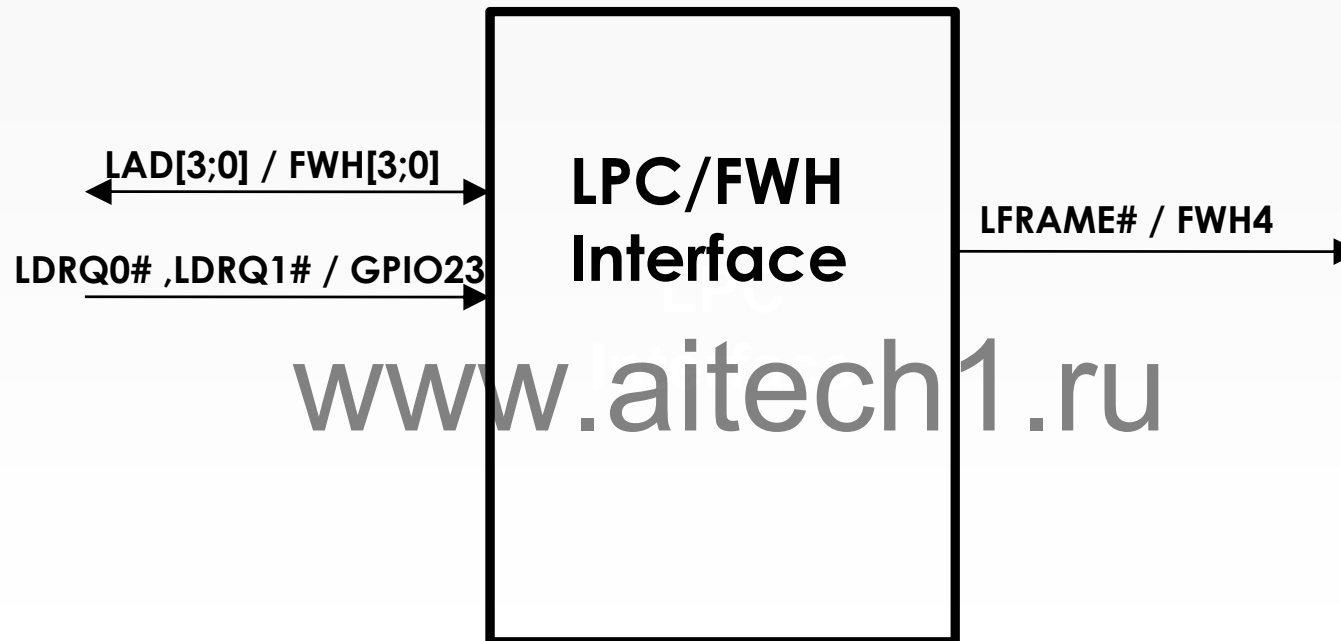
Direct Media Interface Signals



Direct Media Interface Signals Definition

Name	Type	Description
DMI0TXP,DMI0TXN	O	Direct Media Interface Differential Transmit Pair 0
DMI0RXP,DMI0RXN	I	Direct Media Interface Differential Receive Pair 0
DMI1TXP,DMI1TXN	O	Direct Media Interface Differential Transmit Pair 1
DMI1RXP,DMI1RXN	I	Direct Media Interface Differential Receive Pair 1
DMI2TXP,DMI2TXN	O	Direct Media Interface Differential Transmit Pair 2
DMI2RXP,DMI2RXN	I	Direct Media Interface Differential Receive Pair 2
DMI3TXP,DMI3TXN	O	Direct Media Interface Differential Transmit Pair 3
DMI3RXP,DMI3RXN	I	Direct Media Interface Differential Receive Pair 3
DMI_ZCOMP	I	Impedance Compensation Input: Determines DMI input impedance.
DMI_IRCOMP	O	Impedance/Current Compensation Output: Determines DMI output impedance and bias current.

LPC Interface Signals

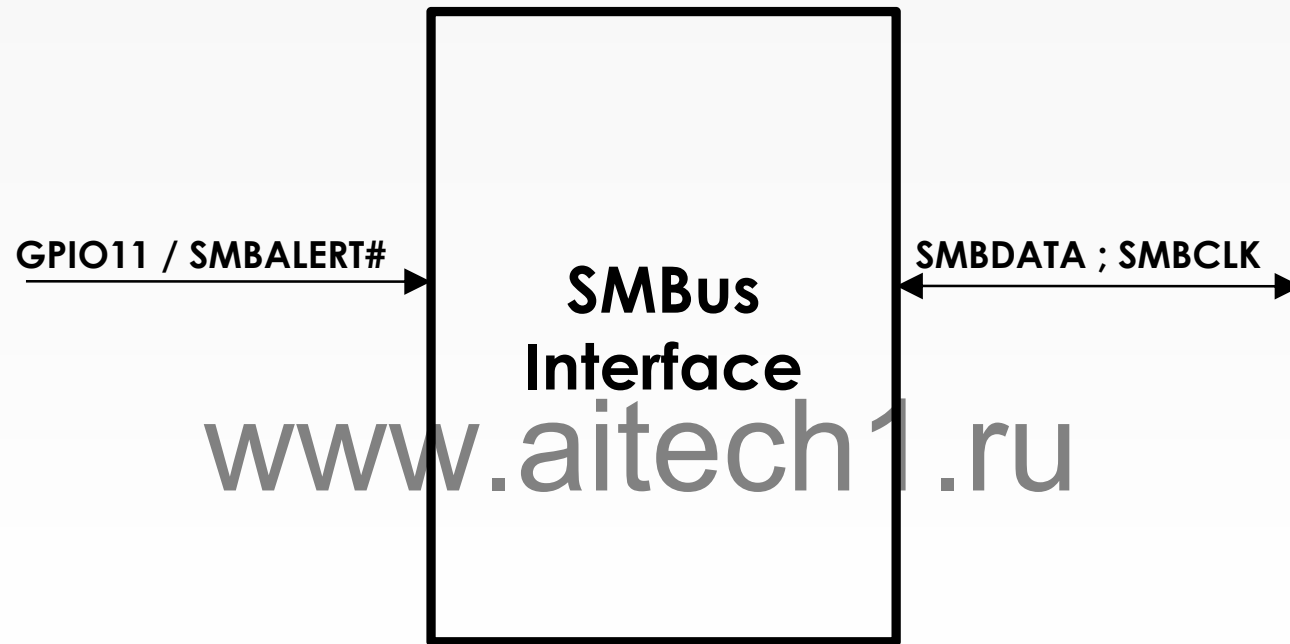


LPC Interface Signals Definition

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	LPC Multiplexed Command, Address, Data: For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH4	O	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0#, LDRQ1# / GPIO23	I	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

www.aitech1.ru

SMBus Interface Signals

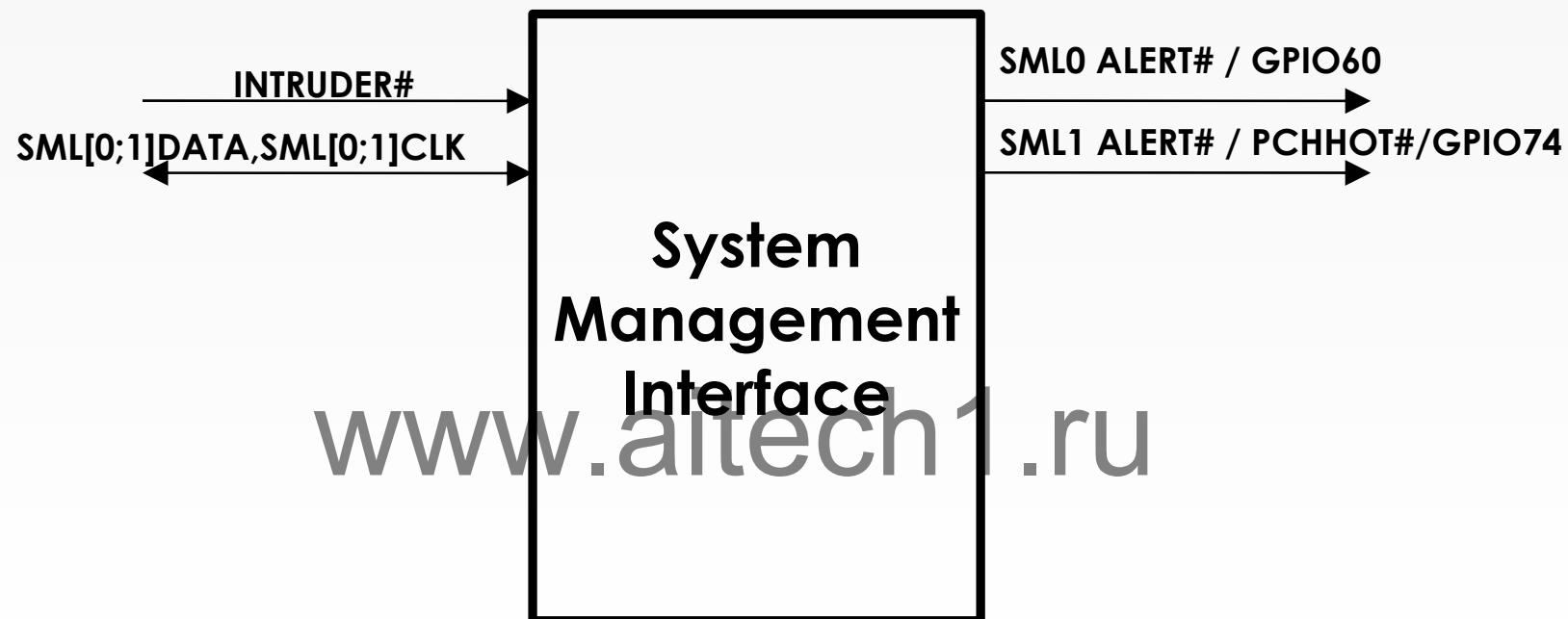


SMBus Interface Signals Definition

Name	Type	Description
SMBDATA	I/OD	SMBus Data: External pull-up resistor is required.
SMBCLK	I/OD	SMBus Clock: External pull-up resistor is required.
SMBALERT# / GPIO11 / (Corporate Only)	I	SMBus Alert: This signal is used to wake the system or generate SMI#. ICH10 Consumer Family: This signal may be used as GPIO11. ICH10 Corporate Family: This signal may be used as GPIO11 or JTAGTDO.

www.aitech1.ru

System Management Interface Signals



System Management Interface Definition

Name	Type	Description
INTRUDER#	I	Intruder Detect: This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SML0DATA	I/OD	System Management Link 0 Data
SML0CLK	I/OD	System Management Link 0 Clock
SML0ALERT# / GPIO60	O OD	SMLink Alert 0: Output of the integrated LAN controller to external PHY.
SML1ALERT# / PCHHOT# / GPIO74	O OD	SMLink Alert 1: Alert for the ME SMBus controller to optional Embedded Controller or BMC. External pull-up resistor is required. This signal can instead be used as PCHHOT# or GPIO74
SML1CLK / GPIO58	I /OD	System Management Link 1 Clock
SML1DATA / GPIO75	I /OD	System Management Link 1 Data

Testability Signals

Name	Type	Description
JTAG_TCK	I	Test Clock Input (TCK): The test clock input provides the clock for the JTAG test logic.
JTAG_TMS	I	Test Mode Select (TMS): The signal is decoded by the Test Access Port (TAP) controller to control test operations.
JTAG_TDI	I	Test Data Input (TDI): Serial test instructions and data are received by the test logic at TDI.
JTAG_TDO	OD	Test Data Output (TDO): TDO is the serial output for test instructions and data from the test logic defined in this standard.

Manageability Signals

Name	Type	Description
SUSWARN# / SUSPWRDNACK /GPIO30 (Mobile Only)	I/O	NOTE: Used by Intel® ME as either SUSWARN# in Deep S4/S5 state supported platforms or as SUSPWRDNACK in non Deep S4/S5 state supported platforms. This signal is in the Suspend power well.
ACPRESENT / GPIO31 (Mobile Only)	I/O	NOTE: Input signal from the Embedded Controller (EC) on Mobile systems to indicate AC power source or the system battery. Active High indicates AC power. This signal is in the Suspend power well.
SATA5GP / GPIO49 / TEMP_ALERT#	I/O	NOTE: Used as an alert (active low) to indicate to the external controller (e.g. EC or SIO) that temperatures are out of range for the PCH or Graphics/Memory Controller or the processor core. This signal is in the Core power well.
GPIO30/ PROC_MISSING (Desktop Only)	I/O	Used to indicate Processor Missing to the Management Engine. NOTE: This signal is in the Suspend power well.

Power and Ground Signals

Name	Description
DcpRTC	Decoupling: This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	Decoupling: Internally generated 1.5 V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	1.05 V Suspend well power. Internal VR mode (INTVRMEN sampled high): Well generated internally. Pins should be left No Connect External VR mode (INTVRMEN sampled low): Well supplied externally. Pins should be powered by 1.05 Suspend power supply. Decoupling capacitors are required. NOTE: External VR mode applies to Mobile Only.
DcpSusByp	Internally generated 1.05 V Deep S4/S5 well power. This rail should not be supplied externally. NOTE: No decoupling capacitors should be used on this rail.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
<u>VccASW</u>	1.05 V supply for the Active Sleep Well. Provides power to the Intel® ME and integrated LAN. This plane must be on in S0 and other times the Intel ME or integrated LAN is used.

Power and Ground Signals

Name	Description
VccDMI	Power supply for DMI. 1.1 V or 1.05 V based on the processor used. Please refer to the respective processor documentation to find the appropriate voltage level.
VccDIFFCLKN	1.05 V supply for Differential Clock Buffers. This power is supplied by the corewell.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. NOTE: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VccIO	1.05 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
<u>VccSus3_3</u>	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccSusHDA	Suspend supply for Intel® HD Audio. This pin can be either 1.5 or 3.3 V.
VccVRM	1.5 V/1.8 V supply for internal PLL and VRMs
VccDFTERM	1.8 V or 3.3 V supply for DF_TVS. This pin should be pulled up to 1.8 V or 3.3 V core.
VccADPLLA	1.05 V supply for Display PLL A Analog Power. This power is supplied by the core well.
VccADPLLB	1.05 V supply for Display PLL B Analog Power. This power is supplied by the core well.
VccADAC	3.3 V supply for Display DAC Analog Power. This power is supplied by the core well.

Power and Ground Signals

Name	Description
VccAClk	1.05 V Analog power supply for internal clock PLL. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLEXP	1.05 V Analog Power for DMI. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLDMI2	1.05 V Analog Power for internal PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAFDIPLL	1.05 V analog power supply for the FDI PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAPLLSATA	1.05 V analog power supply for SATA PLL. This power is supplied by core well. This rail requires an LC filter when power is supplied from an external VR. NOTE: This pin can be left as no connect
V_PROC_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals. Please refer to the respective processor documentation to find the appropriate voltage level.
<u>VccDSW3_3</u>	3.3 V supply for Deep S4/S5 wells. If platform does not support Deep S4/S5 then tie to VccSus3_3.
VccSPI	3.3 V supply for SPI Controller Logic. This rail must be powered when VccASW is powered. NOTE: This rail can be optionally powered on 3.3 V Suspend power (VccSus3_3) based on platform needs.
VccSSC	1.05 V supply for Integrated Clock Spread Modulators. This power is supplied by core well.
VccClkDMI	1.05 V supply for DMI differential clock buffer